

Photonic Flash Soldering on Flex Foils for Flexible Electronic Systems

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Abstract— Ultrathin bare die chips were soldered using a novel soldering technology. Using homogeneous flash light generated by high-power xenon flash lamp the dummy components and the bare die NFC chips were successfully soldered to copper tracks on polyimide (PI) and polyethylene terephthalate (PET) flex foils by using industry standard Sn-Ag-Cu lead free alloys. Due to the selectivity of light absorption, a limited temperature increase was observed in the PET substrates while the chip and copper tracks were rapidly heated to a temperatures above the solder melting temperature. This allowed to successfully soldered components onto the delicate polyethylene foil substrates using lead-free alloys with liquidus temperatures above 200 °C. It was shown that by preheating components above the decomposition temperature of solder paste flux with a set of short low intensity pulses the processing window could be significantly extended compared to the process with direct illumination of chips with high intensity flash pulse. Furthermore, it was demonstrated that with localized tuning of pulse intensity components having different heat capacity could be simultaneously soldered using a single flash pulse.

Keywords—flexible electronics; hybrid integration; soldering; surface mount technology

I. INTRODUCTION

The demand for smart and multi-functional flexible devices has significantly increased in recent years [1]. The need for low-cost and highly reliable integrated systems [2] requires new technological developments. Although simple flexible systems can be fully printed [3], applications with advanced functionality requires developing hybrid systems in which flexible circuitry is combined with surface mount device (SMD) components and silicon-based integrated circuits [4]. Thus, to attain advanced functionality, it is imperative to obtain cost- and time-effective integration of components of complementary functionality into devices on non-standard substrates, such as plastic foils [5],[6]. Substrates for flexible electronics range from copper clad polyimide (PI) foils to polyester foils with copper or printed conductors. Technologies commonly used for interconnecting SMD components include conducting adhesive bonding [6] and oven reflow soldering [7]. The latter process has been successfully employed to integrate

ultra-thin chips onto both rigid and flex substrates [8]. However, reflow soldering technology has certain drawbacks. The requirement of sustaining the whole circuitry above the liquidus temperature of the solder, which is generally above 200 °C, for long holding time makes reflow soldering to be poorly compatible with low-cost flexible foils in roll-to-roll (R2R) settings. The long holding time may cause degradation or deformation of the flexible foil. In fact, when using conventional Sn–Ag–Cu (SAC) lead-free alloys with liquidus temperatures above 200 °C it is impossible to use oven reflow on delicate polyester foils having a maximum processing temperature of around 120 °C – 150 °C. Infrared (IR) light is a recognized alternative [10] to reflow oven soldering allowing soldering components at comparable soldering time. However, the small spot area may require precise positioning of the spot for each component leading to a complex, time-consuming process. Furthermore, applying this technology in a R2R process is challenging as the laser spot needs to align with multiple chips on a moving substrate.

II. PHOTONIC SOLDERING

Recently at Holst Centre we have proposed an alternative approach [11],[12] called photonic soldering. The technology exploits large area illumination generated by a high-intensity light pulse of a flash lamp. The substrate and components having different absorption coefficients lead to selective heating of these elements and ultimately ultrafast (in a range of few milliseconds) soldering of components onto delicate transparent substrates. Advantageously, short timescales limit diffusive heating of the flexible polymer substrate, thereby allowing components to be soldered at temperatures higher than the maximum processing temperature of the foils.

For each component a part of the incident luminous power is absorbed. The total absorbed power, Φ_a , for an incident light with a total incident power of Φ_i and a certain spectrum is equal to [13]

$$\Phi_a = \int \alpha(\lambda) \Phi_{\lambda i} \delta\lambda, \quad (1)$$

where $\alpha(\lambda)$ and $\Phi_{\lambda i}$ are absorbed fraction and the incident spectral power at a certain wavelength λ , respectively. At a given spectrum of the incident light the total absorbed power can be calculated separately for each material. The temperature increase in each material as a function of absorbed energy equals:

$$Q = mc_m\Delta T, \quad (2)$$

where Q is the energy input which is equal to Φ_{α} times the pulse length, m is the mass and c_m is the specific heat of the material. On the one hand, the different material absorption leads to differences in absorbed power and hence selective heating of the components. On the other hand, illumination of electronic devices consisting of multiple components with different heat capacities with a uniform light distribution may lead to differences in heating behavior of these components. In this manuscript the feasibility of photonic flash technology is assessed for soldering multiple components with various heat capacities on flexible foil substrates following the principle illustrated in (Fig. 1b).

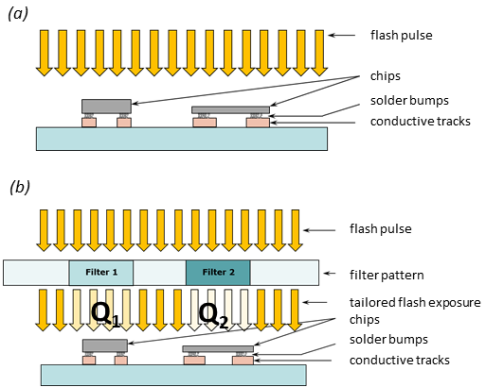


Figure 1. Photonic soldering process. (a) Uniform and (b) tailored for the component's heat capacity through a filter pattern flash pulse directed to the chip placed on printed solder paste.

III. EXPERIMENTAL

A. Materials

A number of different test chip designs were used. Components with four I/Os and 20 I/Os were tested (IZM41 and IZM28 designs from Fraunhofer IZM, Berlin, Germany). The IZM41.1 design is a 1 mm × 1 mm chip with four I/Os (250 μm diameter and 500 μm pitch) and the IZM28 design is a 2.4 mm × 2.4 mm chip with 20 I/Os (100 μm diameter and 300 μm pitch). The chips are bumped with 5 μm Ni/Au at the I/Os. The test chip wafers were diced and thinned to two different thicknesses of 150 μm and 20 μm at DISCO Hi-tech (Kirchheim-bei-München, Germany) by dicing before grinding, followed by a plasma stress relief step. The solder paste used in the study was a lead-free Amtech NC-560-LF Sn96.5Ag3.8Cu0.5 alloy (Inventech, USA) with type 6 size and 85% solid content. Two different flex foils were tested, 50-μm-thick PET foil with 8-μm-thick electroplated copper

(Hanita Coatings, Israel) and 50-μm-thick Upilex-S PI with 13-μm-thick electroplated copper (UBE, Germany). The circuitry was made by wet etching the copper foil. After etching, the copper circuitry was treated with an organic soldering preservative (OSP). With manual stencil printing using a 25 μm stainless steel stencil solder paste was applied on the pads of the measured I/Os. The components were placed with a Dr. Tresky T3200 semiautomatic pick and place machine (Dr. Tresky, Switzerland).

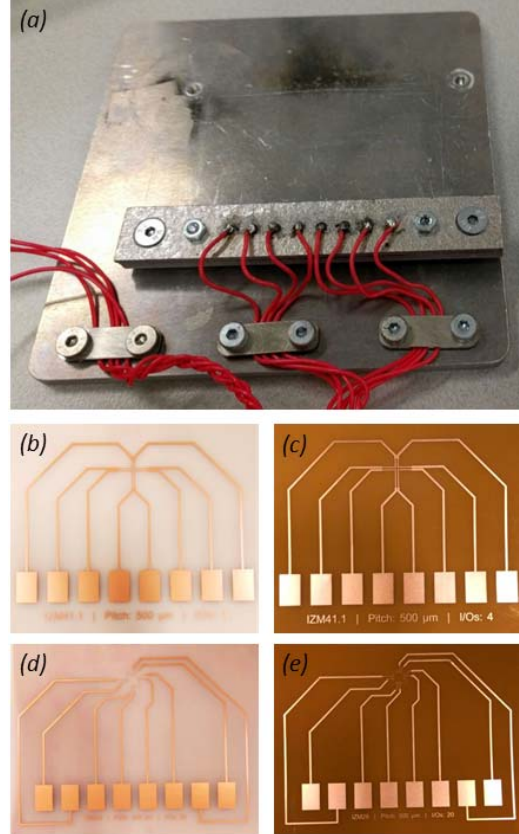


Figure 2. (a) *In situ* four-point resistance measurement probe, and PET-Cu and PI-Cu flex foils for *in situ* characterization of (b-c) IZM 41.1 and (d-e) IZM 28 test chips.

B. Methods

Photonic soldering experiments were performed with a PulseForge 1300 xenon lamp system (Novacentrix, Austin, USA) using pulse energies ranging from 1 J/cm² to 7 J/cm² depending on the component and substrate type. Pulse energies were controlled varying the pulse voltage. The reported energy inputs for each set of pulse parameters were measured with integrated bolometer. For photonic soldering, flex substrates were loaded onto a stainless steel chuck positioned under the center of the xenon lamp. The lamp was positioned 10 mm above the foil surface to insure the uniform energy distribution within absorbed area. For preheating components above the decomposition temperature of solder flux a set of five short 1 ms pulses at pulse energy of 1 J/cm² were used, while a single light pulse with fixed

duration of 5 ms was used to initiate soldering process. The solder joint interconnection resistance is measured *in situ* at 10kHz using the custom developed dual channel four-point probe (Fig. 2). The lead interconnections were located far outside the illumination area to avoid jeopardizing recorded data.

IV. RESULTS AND DISCUSSION

In our earlier work [11] extensive process optimization has been carried out for photonic soldering 20- μm -thick IZM 41.1 and IZM28 test chips both on PET-CU and PI-CU flex substrates. The study indicated there is a narrow process window of pulse energies allowing chips to be photonic soldered on flex foils. While from the lower range pulse energy should be high than certain threshold value in order to sufficiently heat up a chip that would in turn melt solder joints and initiate soldering, there is an upper limit as well. Indeed, at the high end of the energy range either foil deformation or chip removal is observed (Fig. 3). The chip removal is associated with gas formation during the photonic soldering process, possibly originating from decomposition of the solder paste flux.

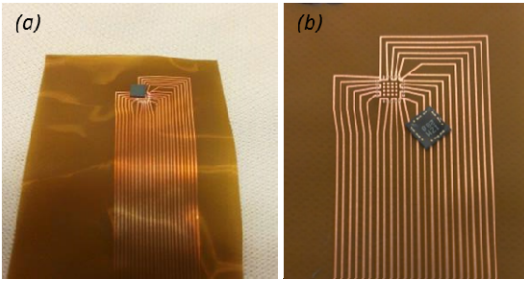


Figure 3. Optical images of 20- μm -thick 2.4 mm \times 2.4 mm chip with 20 I/Os illuminated with excess pulse energies leading to (a) foil deformation and (b) chip removal.

The narrow processing windows [11] identified in our previous work limit the applicability of the photonic soldering technology, especially when aiming for entire circuits being soldered in a single flash. In this work we exploit a dual-stage photonic soldering approach. At the first stage a set of short low intensity pulses, “secondary pulses”, are used to preheat a component above the decomposition temperature of solder paste. The first stage is followed with the “primary” high energy pulse that initiates soldering of the component (Fig. 4).

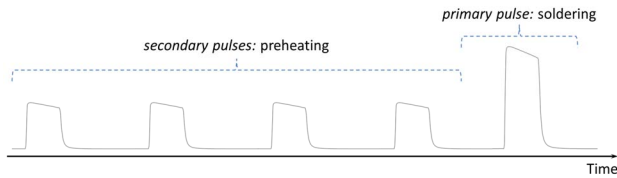


Figure 4. Dual-stage photonic soldering process. A set of short initial low intensity pulses (“secondary pulses”) are used to preheat a component above the decomposition temperature of solder paste flux, while a “primary” high energy pulse initiates soldering of the component.

Fig. 5 shows *in situ* resistance measurement for 20- μm -thick IZM41.1 chip (1 mm \times 1 mm chip with four I/Os) on a PI-Cu foil at a pulse energy of 4.3 J/cm² with and without preheating. While the chip that has been preheating with a set of 5 pulses each with 1 J/cm² has successfully soldered on the flex substrate (Fig. 5a), the chip illuminated directly with 4.3 J/cm² has clearly been overdosed with energy leading to its complete removal from the substrate (Fig. 5b).

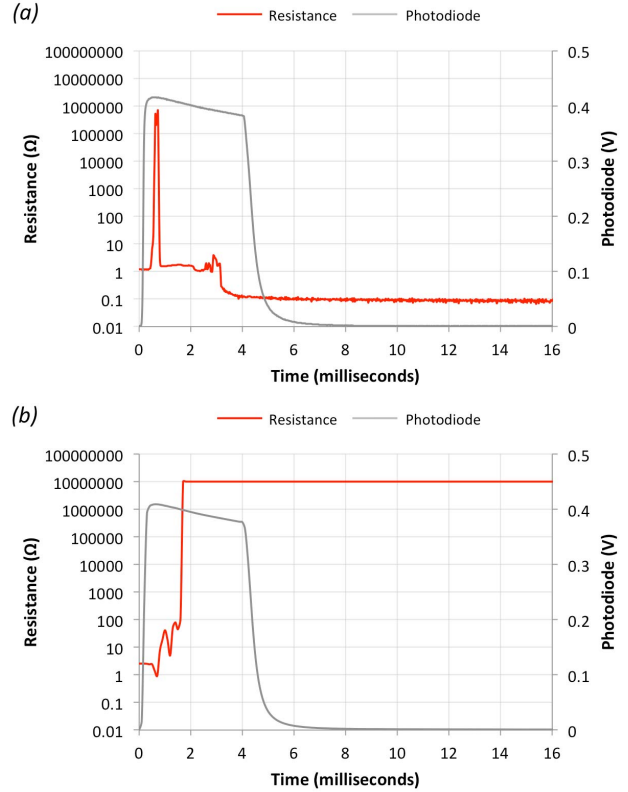


Figure 5. *In situ* resistance measurement for 1 mm \times 1 mm \times 20 μm test chip with four I/Os on PI-Cu foil at a pulse energy of 4.3 J/cm² (a) with and (b) without pre-heating.

The results shown in Fig. 5 point out that gradually increasing temperature of a chip dries the solder paste, which limits gas formation during the photonic soldering process, thereby allowing soldering components at higher pulse energies. Cross section of the solder joint is shown in Fig. 6. Intermetallic layers have been found at between both solder-bond pad as well as solder-Cu tracks interfaces.

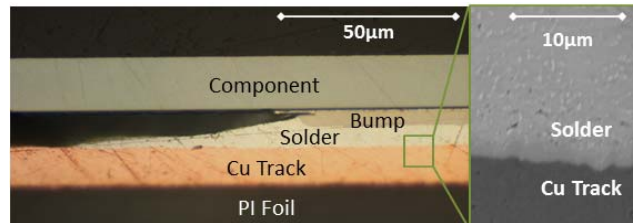


Figure 6. Cross section of solder joint for 20- μm -thick 1 mm \times 1mm chip with 4 I/Os soldered on PI-Cu substrate soldered using 4.3 J/cm² pulse.

To provide a comprehensive verification of the effectiveness of using the dual-stage approach versus direct illumination of the chip using a higher pulse energy, process windows for IZM28 test chips of two different thicknesses (20 μm and 150 μm) on PET-Cu foils were calculated. Tab. 1 provides a comparison between the processing windows of IZM test chips photonicallly soldered on PET-Cu using single- and dual-stage approaches, respectively. For dual-stage experiments a set of 5 pulses at 1 prf each with 1 J/cm² was used to preheat chips above the decomposition temperature of solder flux, while the pulse length of the primary pulse was kept at 5 ms.

TABLE I. PROCESS WINDOW OF SINGLE- AND DUAL-STAGE PHOTONIC SOLDERING PROCESSES FOR 2.4 MM \times 2.4 MM TEST CHIP WITH 20 I/Os AND TWO DIFFERENT THICKNESSES.

Component	Processing window [J/cm ²]	
	Single-stage	Dual-stage
20- μm -thick	2.8 – 3.0	2.7 – 3.5
150- μm -thick	4.8 – 5.0	4.7 – 5.4

The results shown in Tab. 1 point out to a significant extension of the process window for both thin and thick test

chips with the use of secondary pulses. Albeit a significant extension, the processing windows for the two different components do not overlap, hence not allowing for simultaneous photonic soldering of these components. Indeed, at least 4.7 J/cm² is required to solder 150- μm -thick chip on PET-Cu flex foil, while this energy falls way beyond the processing window of 20- μm -thick chip and would certainly cause a severe damage to the thin component. To correct for the aforementioned mismatch in energy levels, a 125- μm -thick kapton film was held between the flash lamp and the thin test chip. Fig. 7 shows *in situ* resistance measurement at a pulse energy of 5.1 J/cm² for 150- μm -thick test with no filter disposed between the flash lamp the chip and thin components covered with kapton film, reducing the incident pulse energy from 5.1 J/cm² to 3.0 J/cm².

In situ resistance probes shown in Fig. 2(b-e) were programmed to obtain two channel output from two sets of I/Os of the same chip (Fig 8a). *In situ* resistance measurement for 2.4 mm \times 2.4 mm test chips with 20 I/Os on PET-Cu foil using the dual channel probe is shown in Fig 8(c) indicating to successful and synchronized soldering of two solder joint clusters at pulse energy of 4.3 J/cm².

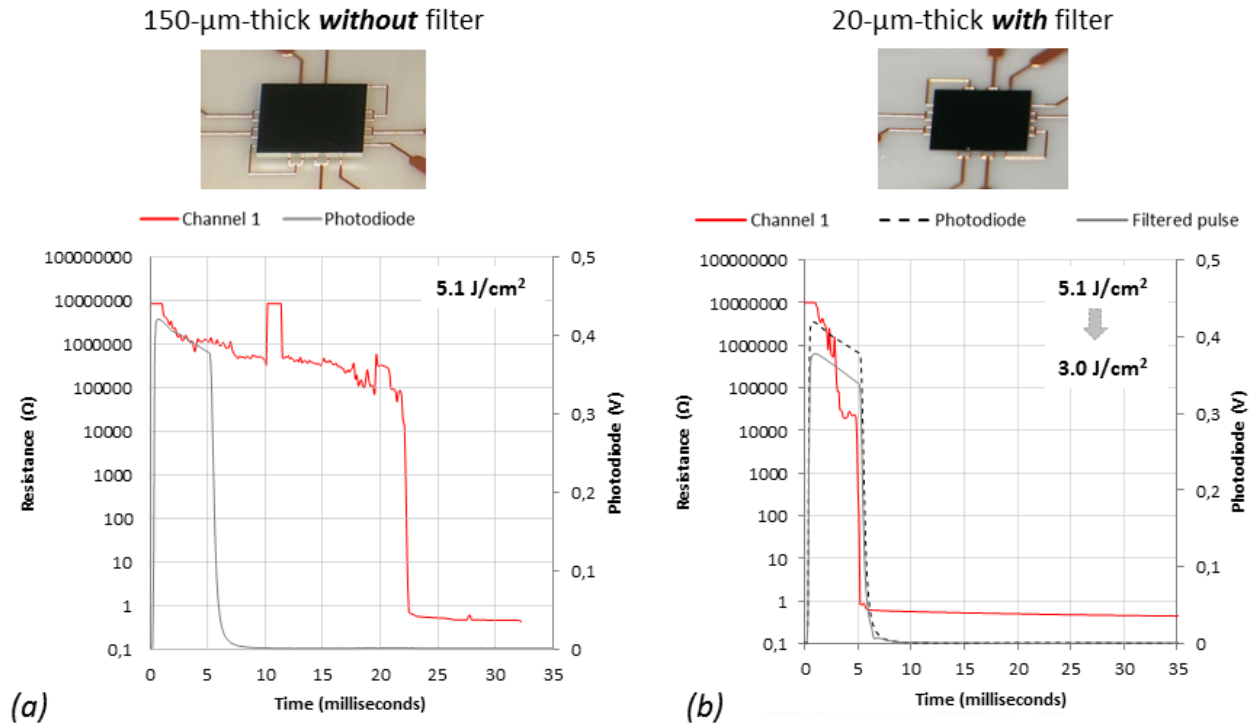


Figure 7. *In situ* resistance measurement for 2.4 mm \times 2.4 mm test chips with 20 I/Os on PET-Cu foil at a pulse energy of 5.1 J/cm². (a) 150- μm -thick chip without filter, (b) 20- μm -thick chip covered with 125- μm -thick kapton film reducing the incident pulse energy from 5.1 J/cm² to 3.0 J/cm².

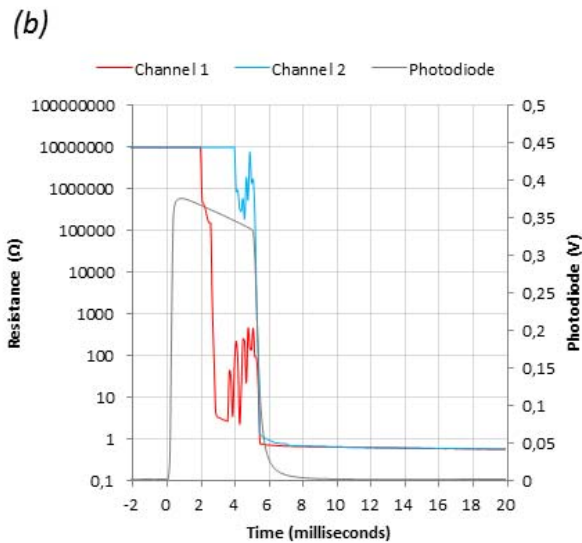
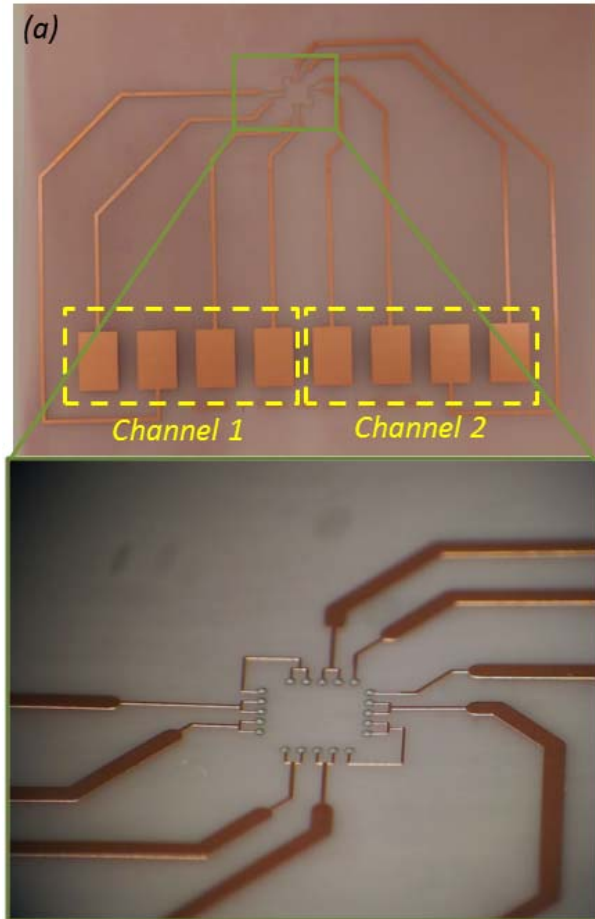


Figure 8. (a) *In situ* dual channel resistance measurement probe for 2.4 mm × 2.4 mm test chips with 20 I/Os on PET-Cu foil with printed solder joints, and (b) *in situ* resistance measurement at a pulse energy of 4.3 J/cm².

For better understanding of photonic soldering process, apart from *in situ* monitoring resistance during soldering process, it is crucial to know what temperatures solder joints reach during the photonic soldering process. To address this

need, a dedicated resistance-temperature (RT) probe has been designed and manufactured on a glass substrate (Fig. 9a-b) allowing *in situ* monitoring of temperature under solder joints with the precision of 0.1°C. Fig 9c shows *in situ* resistance-temperature measurement for 1 mm × 1 mm test chip with 4 I/Os soldered onto a glass RT probe at pulse energy of 4 J/cm². A schematics of the RT probe shown in Fig 9(a) indicates that the temperature probe and solder joints are separated with conductive tracks. Therefore, temperature readouts shown in Fig 9(c) could only serve as indicative numbers to what temperatures solder joints reach during the process. However, owing to high conductivity of printed thin silver tracks, it could be assumed that temperature of solder joints during soldering process should not much vary from the obtained temperatures under conductive tracks.

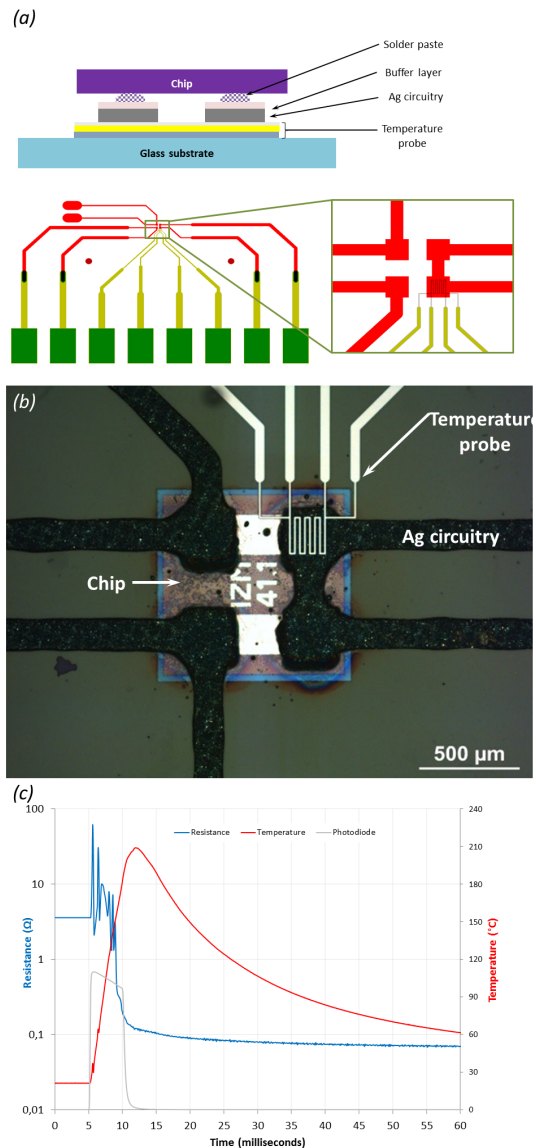


Figure 9. (a) A schematics of the resistance-temperature (RT) probe with a chip placed on printed solder joints, (b) backside microseopic image of 1 mm × 1 mm test chip with 4 I/Os soldered onto a glass RT probe, and (c) *in situ* resistance-temperature measurement at pulse energy of 4 J/cm².

To provide a verification of feasibility of applying photonic technology for soldering functional elements to flex foils, the 2.0 mm × 1.5 mm NFC radio chip (ST Microelectronics M24LR64-R) with 10 I/Os has been successfully soldered to PI-Cu foil with energy pulse of 3.9 J/cm² (Fig. 10). Fig. 10(b-c) shows a sequence of video frames illustrating NFC readout of the tag with a smartphone.

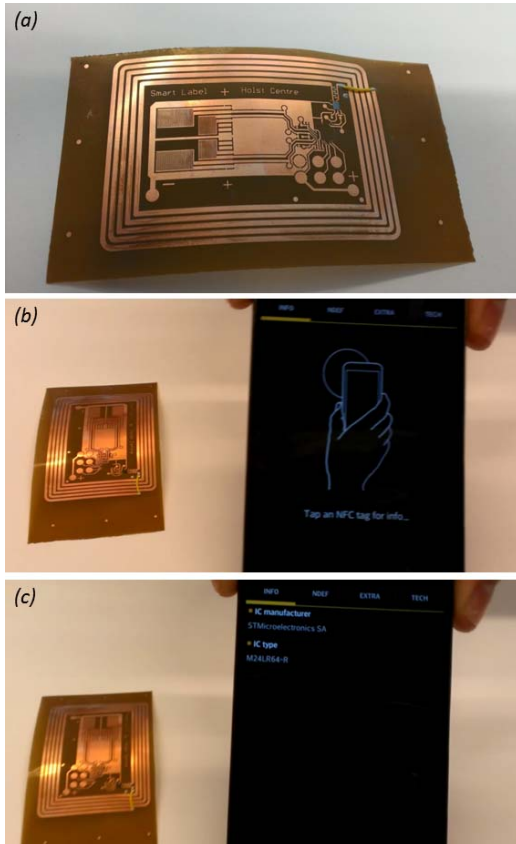


Figure 10. (a) PET-Cu RFID smart label with 2.0 mm × 1.5 mm NFC radio chip (20- μ m-thick, 10 I/Os) soldered with energy pulse of 3.9 J/cm². (b)-(c) NFC readout of with a smartphone

V. CONCLUSIONS

The possibility of soldering various components on flexible circuits using photonic technology provides a possibility for creating circuits with advanced functionality using a roll-to-roll compatible process. It has been shown that thin dummy bare die chips could be soldered to copper circuits on flex foils in several milliseconds using photonic soldering technology. It has also been shown that apart from significantly reducing soldering time, the photonic soldering technique can be applied for soldering using a conventional SAC alloy on delicate low-cost PET foils, which is not possible with reflow oven soldering. Furthermore, it has been shown that using a filter mask disposed between the flash lamp multiple chips having different heat capacity could be exposed with the matching light intensities and thereby could be soldered using a (single) light pulse. It has

been demonstrated that 2.4 mm × 2.4 mm bare die chips of two different thicknesses (20 μ m and 150 μ m) could be simultaneously soldered with a single 5 ms flash pulse. Apart from *in situ* monitoring resistance during the photonic soldering process, using the specially designed temperature-resistance glass probe both temperature and resistance of solder joints has been measured in-line. An applicability of developed photonic soldering technology for soldering functional elements on flex foils using industry standard lead-free SAC alloys has been demonstrated by soldering NFC radio chip to PI-Cu smart label. The prospects of using photonic soldering technology in combination with a filter mask makes it an advantageous mass production approach for entire circuits on low-cost flex foils being soldered in a single flash.

ACKNOWLEDGMENT

The authors thank Dr. M. Cauwe (Imec CMST) in supplying the PET and PI foil circuits with electroplated copper and R. Kusters, Dr. E. Smits and M. Giesbers (Holst Centre) for fruitful discussions.

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